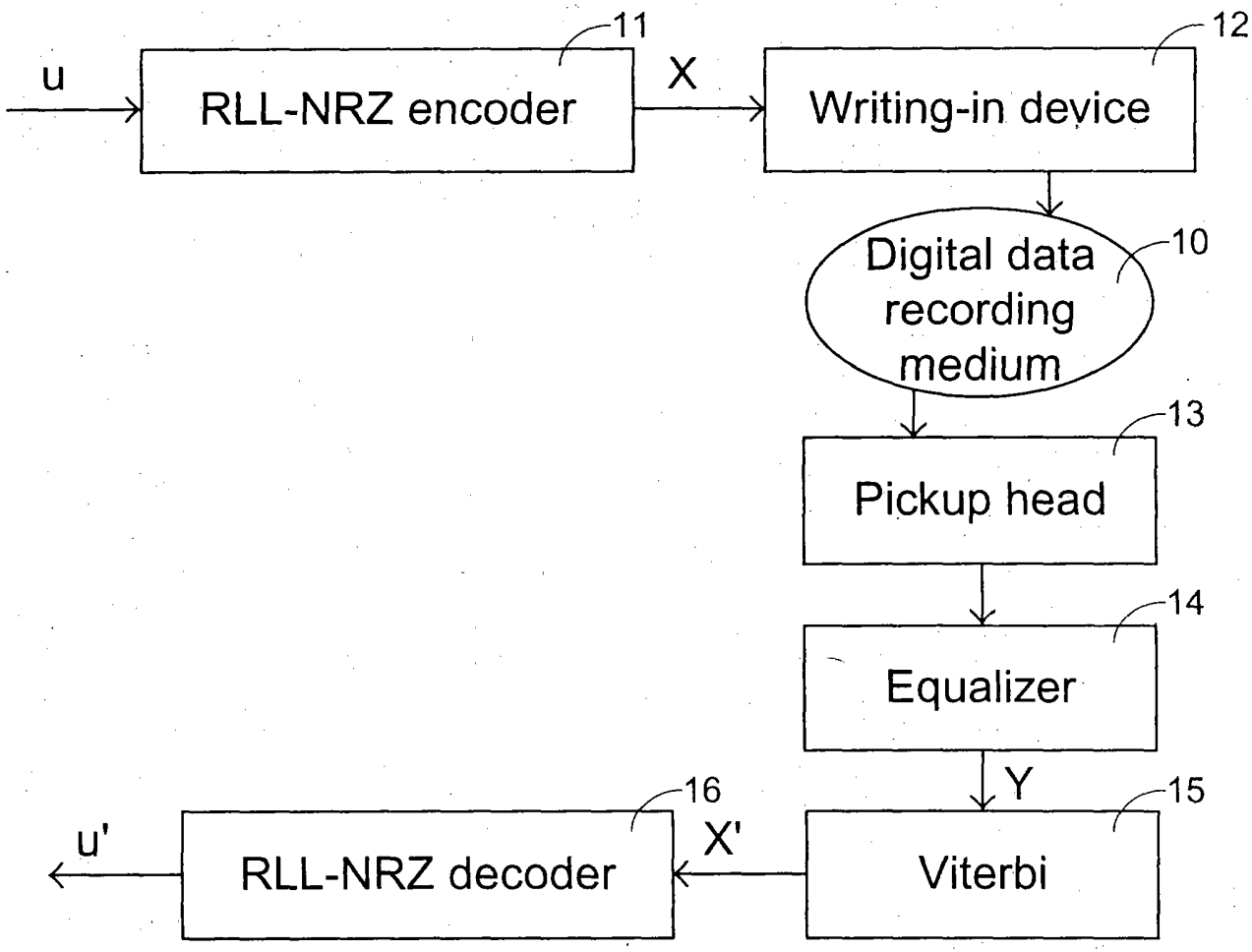

Fig.1
PRIOR ART

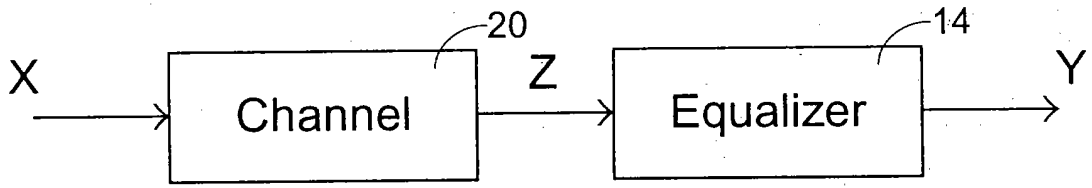

Fig.2
PRIOR ART

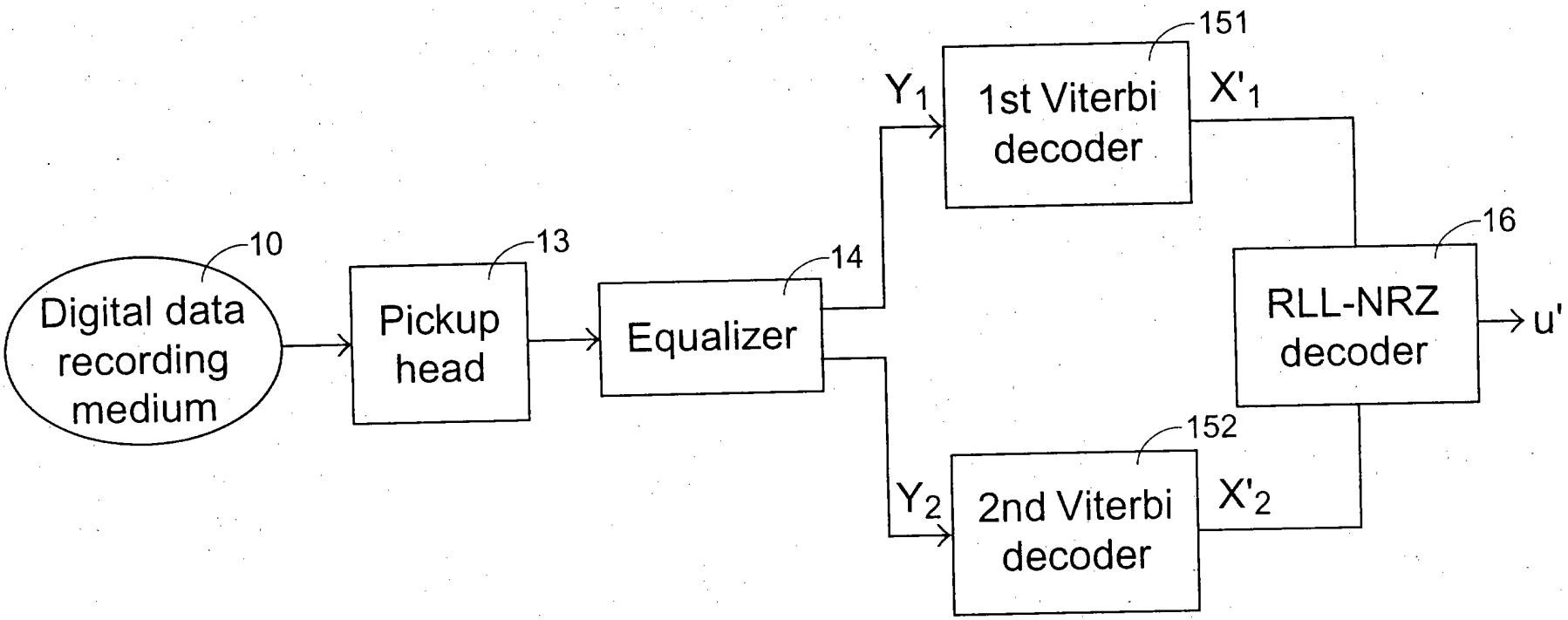

Fig.3
PRIOR ART

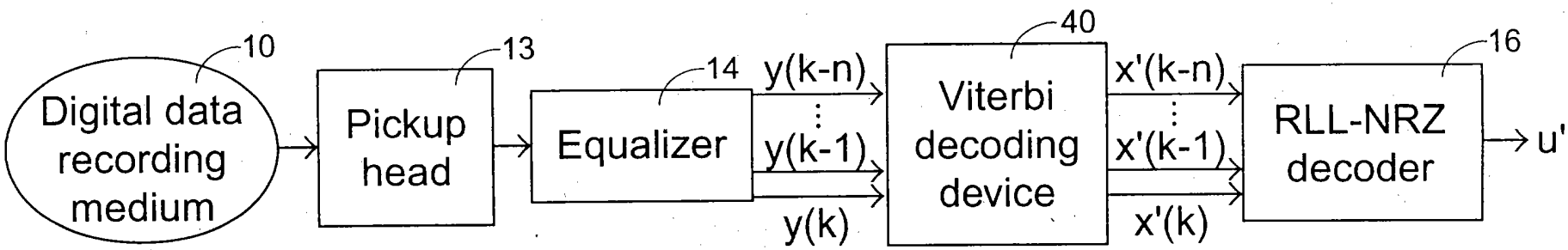
10
Digital data recording medium
13
Pickup head
14
Equalizer
y(k-n)
y(k-1)
y(k)
40
Viterbi decoding device
x'(k-n)
x'(k-1)
x'(k)
16
RLL-NRZ decoder
u'

Fig.4

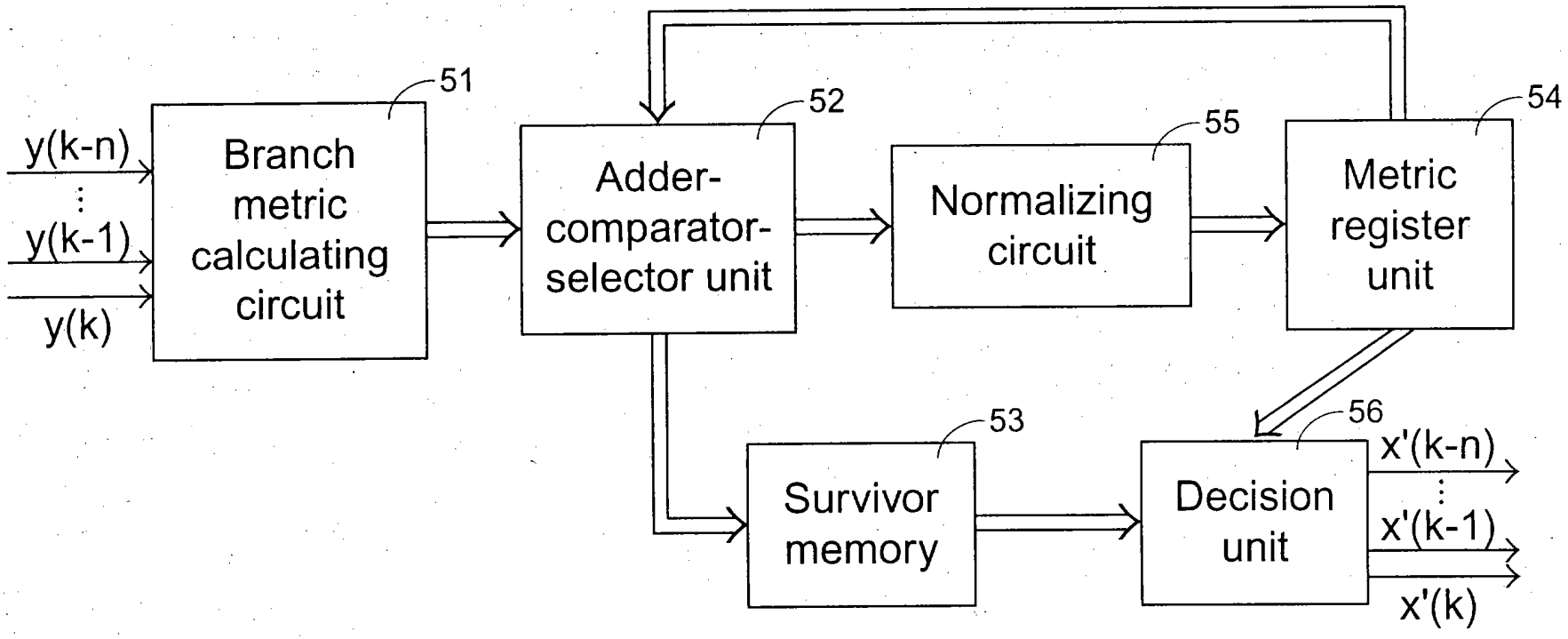
y(k-n)
y(k-1)
y(k)
Branch metric calculating circuit
51
Adder-comparator-selector unit
52
Normalizing circuit
55
Metric register unit
54
Survivor memory
53
Decision unit
56
x'(k-n)
x'(k-1)
x'(k)

Fig.5

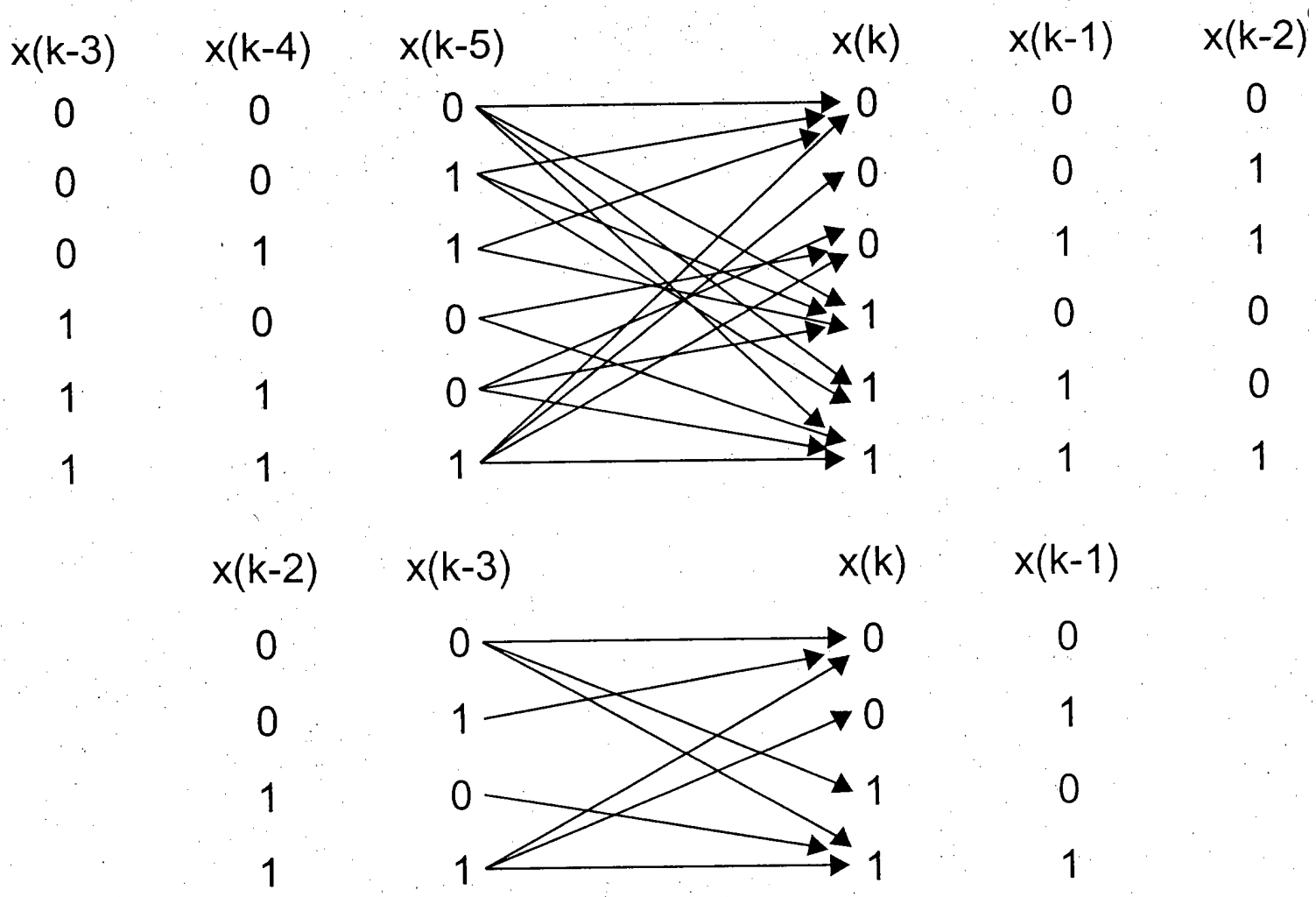
x(k-3)
x(k-4)
x(k-5)
x(k)
x(k-1)
x(k-2)
0 0 0 0 0 0
0 0 1 0 0 1
0 1 1 0 1 1
1 0 0 1 0 0
1 1 0 1 1 0
1 1 1 1 1 1
x(k-2)
x(k-3)
x(k)
x(k-1)
0 0 0 0
0 1 0 1
1 0 1 0
1 1 1 1

Fig.6A

x(k-2) x(k-3)	x(k) x(k-1)	y(k)	y(k-1)
0(-0.5) 0(-0.5)	0(-0.5) 0(-0.5)	-2	-1.5
0(-0.5) 1(0.5)	0(-0.5) 0(-0.5)	-1	0
1(0.5) 1(0.5)	0(-0.5) 0(-0.5)	0	1
1(0.5) 1(0.5)	0(-0.5) 1(0.5)	1	1.5
0(-0.5) 0(-0.5)	1(0.5) 0(-0.5)	-1	-1.5
0(-0.5) 0(-0.5)	1(0.5) 1(0.5)	0	-1
1(0.5) 0(-0.5)	1(0.5) 1(0.5)	1	0
1(0.5) 1(0.5)	1(0.5) 1(0.5)	2	1.5

Fig.6B

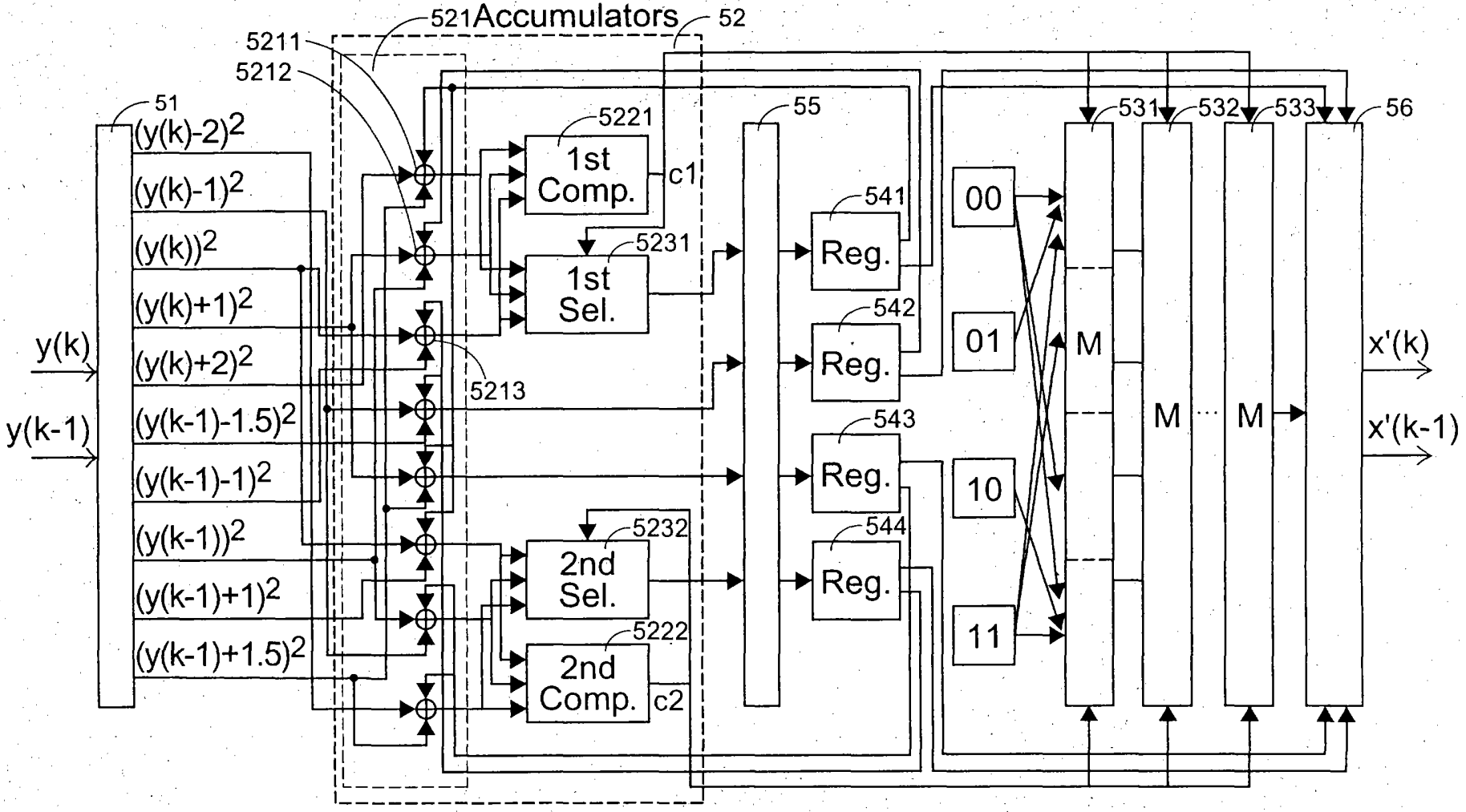
521Accumulators
52
5211
5212
51
(y(k)-2)2
(y(k)-1)2
(y(k))2
(y(k)+1)2
(y(k)+2)2
(y(k-1)-1.5)2
(y(k-1)-1)2
(y(k-1))2
(y(k-1)+1)2
(y(k-1)+1.5)2
y(k)
y(k-1)
5213
5221
1st Comp.
c1
5231
1st Sel.
5232
2nd Sel.
5222
2nd Comp.
c2
55
541
Reg.
542
Reg.
543
Reg.
544
Reg.
00
01
10
11
531
532
533
56
M
M
M
x'(k)
x'(k-1)

Fig.7